FUZZY LOGIC NEURAL PROCESSOR

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Abstract: An architecture of fuzzy logic neural processor is discussed.
General structure of fuzzy logic neural processor based on t-norm and t-conorm is proposed.

1. Introduction.

An intention of this paper is to outline of a highly parallel architecture of a fuzzy logic dynamic neural processor. Our discussion is based on a theory of fuzzy logic neurons sketched in [1], and [2].

2. Architecture of fuzzy logic neural processor.

In [1] the dynamic behavior of the neuron has been shaped as follows

$$\begin{cases} X_{n+1} = X_n \circ R_1 \,\Delta\, U_n^1 \circ R_2 \,\Delta\, U_n^2 \circ R_3 \\ Y_n = X_n \circ R_4 \,\Delta\, U_n^1 \circ R_5 \,\Delta\, U_n^2 \circ R_6 \end{cases} \tag{1}$$

An architecture of fuzzy logic neural processor is depicted in Figure 1.

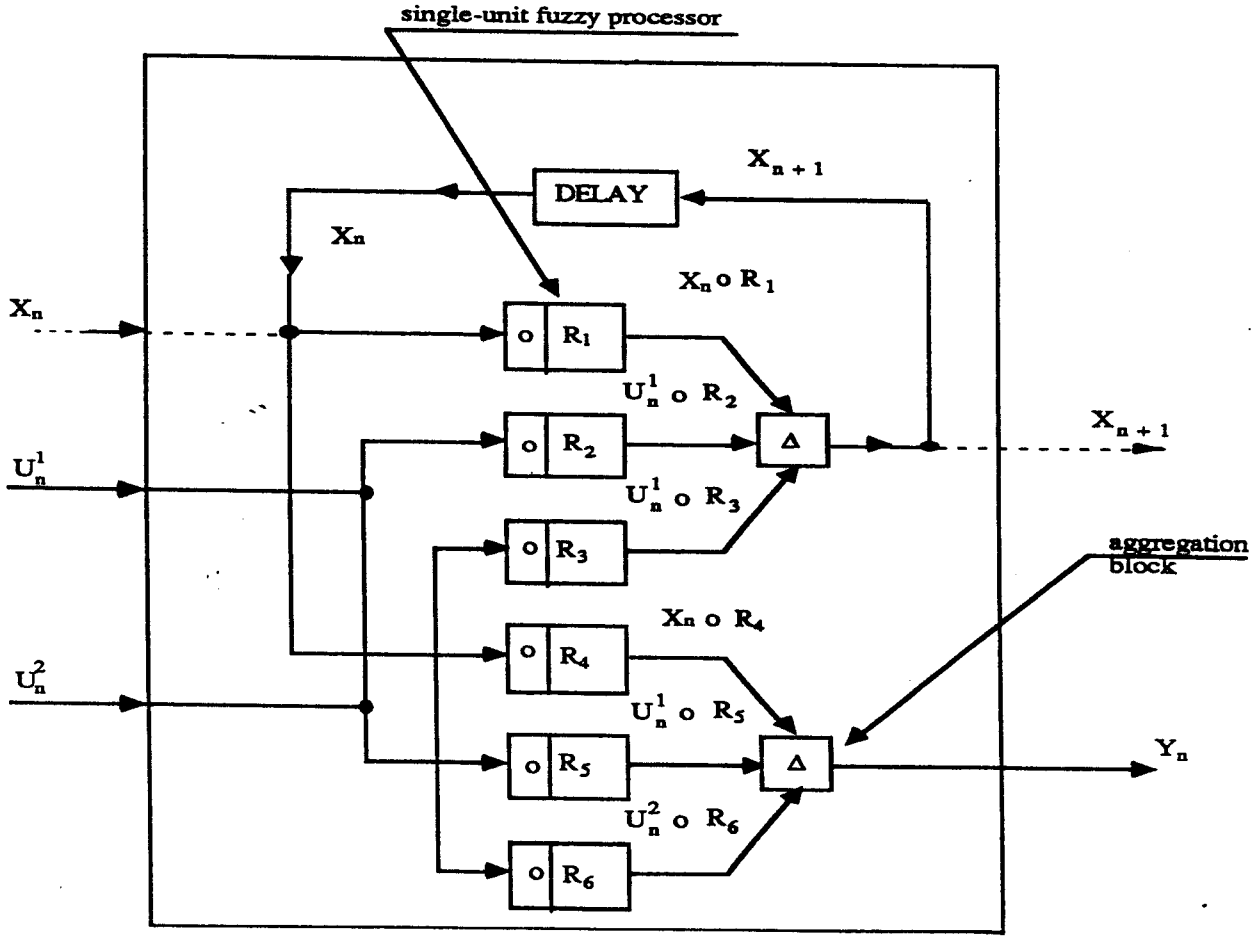

Figure 1. Architecture of dynamic fuzzy neuron.

It is interesting to note that the fuzzy neuron consists of six single-unit fuzzy processors R_1, R_2, R_3, R_4, R_5, and R_6; two contribution blocks Δ, and delay block.

One should note that the above configuration processes fuzzy information dynamically in parallel mode using only three basic blocks.

It is worth to investigate a nature of a single-unit fuzzy neuron processor. Viewing into a nature of a neuron it is worth to recall that a highly nonlinear property with a flexible saturation must be considered. Thinkging of the above paradigm and Equation (1) we propose the following model of a single-unit fuzzy neuron processor R_1.

$$X_{n+1} = X_n \circ R_1, \quad n = 0, 1, 2, 3, \ldots$$

where

$$R_1 = \bigwedge_{i=1}^{I} \begin{cases} 1, & X_{n(i)} \le X_{n+1(i)} \\ X_{n(i)}, & X_{n(i)} > X_{n+1(i)} \end{cases}$$

therefore

$$X_{n+1} = \bigvee_{X} \left[X_n \wedge \bigwedge_{i=1}^{I} \begin{cases} 1, & X_{n(i)} \le X_{n+1(i)} \\ X_{n(i)}, & X_{n(i)} > X_{n+1(i)} \end{cases} \right]$$

and finally

$$X_{n+1} = \bigvee_{X} \left[\bigwedge_{i=1}^{I} \begin{cases} 1, & X_{n(i)} \le X_{n+1(i)} \\ X_n \wedge X_{n(i)}, & X_{n(i)} > X_{n+1(i)} \end{cases} \right] \tag{2}$$

A block diagram architecture in terms of mathematical operations of the single-unit fuzzy neuron processor is depicted in Figure 2.

It consists of a logic gate "equal or less than ≤", a "min-aggregation gate $\bigwedge_i$", and a "sup-gate $\bigvee_X$".

It is worth to stress that a basic building block of any dynamic fuzzy neuron is expressed by Equation (2) and dipicted in Figure 2.

It remains to say that the single-unit fuzzy neuron processor exhibits a highly parallel architecture.

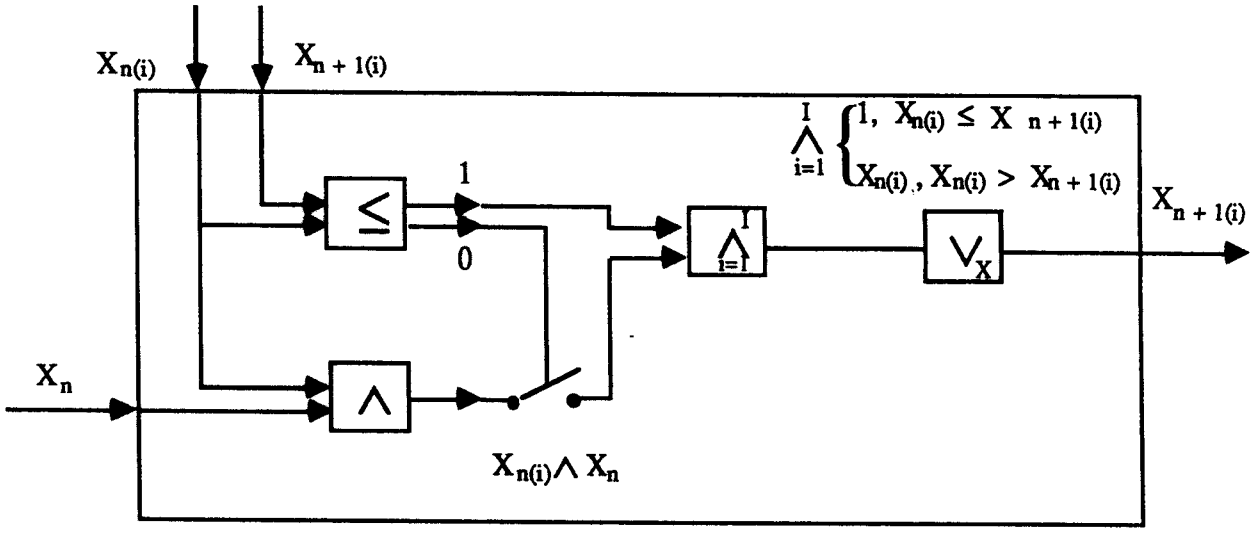

Figure 2. A block-diagram architecture of a single-unit fuzzy neruon processor R_1.

3. Generalized structure of fuzzy logic processor.

In general any fuzzy static neuron with 2 inputs and 1 output can be formulized by the following

$$Y = X_1 * \left\{ \textcircled{a}_{i=1}^{I} \left[X_{1(i)} \textcircled{b} Y_{(i)} \right] \right\} \Delta$$
$$\Delta X_2 * \left\{ \textcircled{a}_{i=1}^{I} \left[X_{2(i)} \textcircled{b} Y_{(i)} \right] \right\} \qquad (3)$$

where * denotes a generalized inference operator, (a) is a generalized aggregation operator, (b) is a generalized implication operator, and Δ denotes a generalized contribution operator.

Equation (3) can be extended to M-inputs fuzzy neuron as follows

$$Y = \underset{k=1}{\overset{M}{\Delta}} \left\{ X_K * \left[\underset{i=1}{\overset{I}{(a)}} \left[X_{K(i)} (b) Y_{(i)} \right] \right] \right\} \tag{4}$$

where $k = 1, 2, 3, \ldots, M$ is the number of inputs.

Triangular norms and their dual triangular conorms could be used to generate the aggregation operator Δ, the composition operator *, and the contribution operators (a).

Consequantly in terms of t-norm and t-conorm, the M-input fuzzy neuron (4) may be expressed as

$$Y = \underset{K=1}{\overset{M}{T}} \left\{ \underset{X}{S} \left[X_K \, T \left[\underset{i=1}{\overset{I}{S}} \left(X_{K(i)} (b) Y_{(i)} \right) \right] \right] \right\} \tag{5}$$

where T stands for t-norm, and S denotes t-conorm.

General architecture of M-input fuzzy neuron in terms of t-norm, t-conorm and implication operator is depicted in Figure 3.

The generalized architecture of the fuzzy neuron consists of : an implication gate (b), a t-norm aggregation gate (s), and t-conorm gate $\hat{T}$, an inf-conorm gate (S) and a t-conorm gate (T).

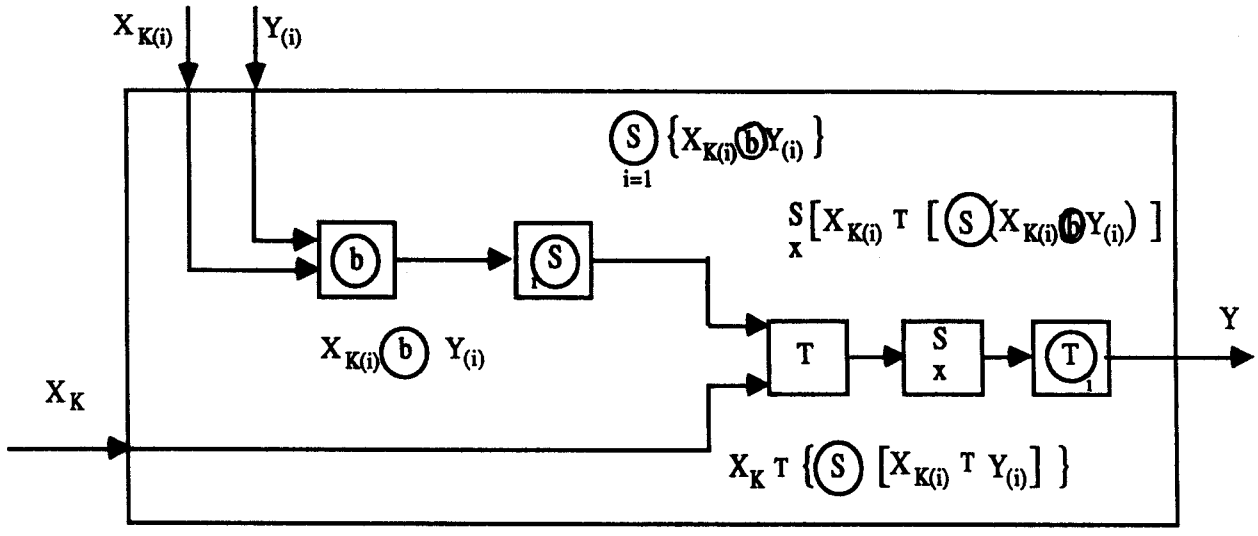

Figure 3. Generalized architecture of M-input fuzzy neuron.

4. Summary.

An architecture of fuzzy logic neural processor has been proposed. This investigation may have an impact on VLSI implementation of fuzzy logic neural systems.

References.

[1] J. Kiszka, M.M. Gupta, Fuzzy logic model of single neuron, BUSEFAL, 1989.

[2] J. Kiszka, M. Gupta, Fuzzy logic neural network, BUSEFAL, 1989.